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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/062,992	01/31/2002	Steven Teig	SPLX.P0096	2859

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EXAMINER

LU, KUEN S

ART UNIT PAPER NUMBER

2167

DATE MAILED: 07/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/062,992	TEIG ET AL.	
	Examiner	Art Unit	
	Kuen S. Lu	2167	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 May 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 and 3-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 and 3-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Reopened Prosecution

1. The Action is responsive to Applicant's Appeal Brief, filed July 5, 2005.
2. In view of the Pre-Appeal Brief Request for Review filed May 15, 2006, prosecution is hereby reopened. A new ground of rejection is set forth below.
3. To avoid abandonment of the application, Appellant must exercise one of the two options:
 - 3.1 file a reply under 37 CFR 1.111 (if this Office Action is non-final rejection); or
 - 3.2 request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. Please see 37 CFR 1.193(b)(2).

Claim Rejections - 35 USC § 101

4. 35 U.S.C. § 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

- 4.1. Claims 1 and 3-21 are rejected under 35 U.S.C. § 101 because the claimed invention is directed to non-statutory subject matter.

As set forth in MPEP 2106 (II) (A):

The claimed invention as a whole must accomplish a practical application. That is, it must produce a "useful, concrete and tangible result." State Street, 149 F.3d at 1373, 47 USPQ2d at 1601-02. The purpose of this requirement is to limit patent protection to inventions that possess a certain level of "real world" value, as opposed to subject matter that represents nothing more than an idea or concept, or is simply a starting point for future investigation or research (Brenner v. Manson, 383 U.S. 519, 528-36, 148 USPQ 689, 693-96); In re Ziegler, 992, F.2d 1197, 1200-03, 26 USPQ2d 1600, 1603-06 (Fed. Cir. 1993)).

Accordingly, a complete disclosure should contain some indication of the practical application for the claimed invention, i.e., why the applicant believes the claimed invention is useful.

Apart from the utility requirement of 35 U.S.C. 101, usefulness under the patent eligibility standard requires significant functionality to be present to satisfy the useful result aspect of the practical application requirement. See *Arrhythmia*, 958 F.2d at 1057, 22 USPQ2d at 1036. Merely claiming nonfunctional descriptive material stored in a computer-readable medium does not make the invention eligible for patenting. For example, a claim directed to a word processing file stored on a disk may satisfy the utility requirement of 35 U.S.C. 101 since the information stored may have some "real world" value. However, the mere fact that the claim may satisfy the utility requirement of 35 U.S.C. 101 does not mean that a useful result is achieved under the practical application requirement. The claimed invention as a whole must produce a "useful, concrete and tangible" result to have a practical application.

As per claim 1, the claimed invention is a description of an abstract data structure without showing any practical application.

As per claim 11, the claimed invention is a combination of a description of an abstract data structure and an abstract methodology for accessing and retrieving data structure.

The claimed invention as described in claims 1 and 11 are not supported by either an asserted or a well-established utility and shows no useful or concrete results as required for a practical application test. Consequence is non-statutory.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. § 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

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5.1. Claim 1 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 1, it recites a phrase describing a data structure for storing sub-networks without claim elements for particularly pointing out the subject matter of the invention.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6.1. Claims 1, 11, 20 and 21 are rejected under 35 U.S.C. 102(b) as anticipated by Trimberger (U.S. Patent 5,959,881).

As per claim 1, Trimberger teaches "A data storage structure that stores a plurality of sub-networks," (See Fig. 3 and col. 6, line 42 - col. 7, line 28 where a configurable logic block equips with memory to store logic functions and control sections among other sub-networks) "wherein each sub-network performs at lease three output functions," (See Fig. 3 and col. 6, line 42 - col. 7, line 28 where control section performs output functions Ds, F and G) "wherein the data storage stores each sub-network indexed by a

parameter derived from all output functions of the sub-network" (See Fig. 3, col. 5, lines 59-67 and col. 6, line 42 - col. 7, line 28 where the configurable logic block stores the control section output functions having the inputs for flip-flop inputs supplied by outputs of the lookup tables associated with functional generators and control inputs, and user logic data is stored into and retrieved from memory where subset of data identifiable and retrievable).

As per claim 11, Trimberger teaches "A sub-network management system" (See col. 7, lines 42-51 where a programmable logic device is programmed by using a library of elements) comprising:

"a data storage structure that stores a plurality of sub-networks," (See Fig. 3 and col. 6, line 42 - col. 7, line 28 where a configurable logic block equips with memory to store logic functions and control sections among other sub-networks) "wherein each sub-network is for performing at lease three output functions," (See Fig. 3 and col. 6, line 42 - col. 7, line 28 where control section performs output functions Ds, F and G) "wherein the data storage stores each sub-network indexed by a parameter derived from all output functions of the sub-network" (See Fig. 3 and col. 6, line 42 - col. 7, line 28 where the configurable logic block stores the control section output functions having the inputs for flip-flop inputs supplied by outputs of the lookup tables associated with functional generators and control inputs); and

"a data access manager that identifies and retrieves sub-networks from the data storage structure" (See Fig. 3 and col. 6, line 42 - col. 7, line 28 where the flip-flops of the configurable logic block access and retrieve the outputs of functional generators).

As per claims 20 and 21, Trimberger teaches "at least some of the sub-networks comprise a first circuit having a first output outside the sub-network and a second circuit having a second output outside the sub-network, wherein the first circuit receives a direct or indirect input from the second circuit" (See Fig. 3 and col. 6, line 42 - col. 7, line 28 where the second output of the sub-network G extends outside of the configurable logic block and connects to elements 313/314, and the first output of the sub-network F is an input to the sub-network which extends outside of the configurable logic block and connects elements 319/320).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7.1. Claims 3-7, 10 and 12-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Trimberger (U.S. Patent 5,959,881), as applied to claims 1 and 11 above, and in view of Pedersen et al. (U. S. Patent 6,134,705, hereafter "Pedersen").

As per claim 3, Trimberger teaches "each sub-network includes a set of circuit elements" (See Fig. 3 and col. 6, line 42 - col. 7, line 28 where the flip-flops, functional generator and control sections are among the circuit elements in the configurable logic block).

Trimberger does not explicitly teach "the data storage structure stores each sub-network in terms of (i) an encoding of a graph that represents the topology of the set of circuit elements of each sub-network, wherein the graph includes a node for each circuit element of the sub-network".

However, Pedersen teaches "the data storage structure stores each sub-network in terms of (i) an encoding of a graph that represents the topology of the set of circuit elements of each sub-network, wherein the graph includes a node for each circuit element of the sub-network" (See col. 6, lines 20-23 where electronic design is provided as a high level Boolean representation, encoded in a hardware design language and as schematic or any other form representing the logical arrangement of a device, and at col. 1, lines 37-43 referencing U.S. Patent Application 08/958,778 where Southgate states a fully described block diagram stored in a graphic design file at col. 4, lines 65-67).

It would have been obvious to one having ordinary skill in the art at the time of the

applicant's invention was made to combine Pedersen's teaching with Trimberger reference by applying the techniques of incremental compiling to programming circuit design because both references are directed to circuit design where Trimberger teaches method for properly reducing number of library elements while Pedersen teaches method for efficiently delineating circuit design changes, and the combined teaching would have provided a method for both efficiently and correctly verifying and identifying the design of integrated circuit having an optimal number of library elements.

The combined teaching of the Pedersen and Trimberger references further teaches "(ii) a set of local functions that includes a local function for each node of the graph" (See Pedersen: Fig. 7E where a set of local functions include the functions at nodes u and v).

As per claim 12, Trimberger teaches data structure storing sub-networks as previously described in claim 11 rejection above.

Trimberger does not explicitly teach "the data access manager receives a parameter, the manager searches the data storage structure for sub-networks that are stored based on the received parameter, and if the manager finds a sub-network that is stored based on the received parameter, the manager retrieves the sub-network".

However, Pedersen teaches "the data access manager receives a parameter, the manager searches the data storage structure for sub-networks that are stored based on the received parameter, and if the manager finds a sub-network that is stored based on the received parameter, the manager retrieves the sub-network" (See Pedersen: Fig.

3A, step 314, and col. 10, lines 43-50 where user input the changed design for receiving and retrieving the sub-netlist to be incrementally recompiled).

It would have been obvious to one having ordinary skill in the art at the time of the applicant's invention was made to combine Pedersen's teaching with Trimberger reference by applying the techniques of incremental compiling to programming circuit design because both references are directed to circuit design where Trimberger teaches method for properly reducing number of library elements while Pedersen teaches method for efficiently delineating circuit design changes, and the combined teaching would have provided a method for both efficiently and correctly verifying and identifying the design of integrated circuit having an optimal number of library elements.

As per claim 4, the combined teaching of the Pedersen and Trimberger references further teaches "the data storage structure stores, for each sub-network, an identifier that specifies the set of local functions and the graph" (See Pedersen: col. 11, line 62 – col. 4, line 3 where a sub-netlist is identified and synthesized for its nodes and the graph by mapping the changed design onto the target hardware).

As per claim 5, the combined teaching of the Pedersen and Trimberger references further teaches "the identifier for each sub-network specifies the locations that store the set of local functions and the graph of the particular sub-network" (See Pedersen: Figs. 4A-4B and at col. 11, line 62 – col. 4, line 3 where a sub-netlist is identified and

synthesized for its nodes and the graph by mapping the changed design onto the target hardware).

As per claims 6 and 16, the combined teaching of the Pedersen and Trimberger references further teaches "the identifier for each sub-network is a set of indices that specifies the set of local functions and the graph of the sub-network" (See Pedersen: Figs. 4A-4B and col. 11, lines 62-66, col. 12, lines 10-15 and 43-45, and col. 13, lines 28-38 and 43-54 where an identified sub-netlist is analyzed for its gates locations and nodes functions).

As per claims 7 and 17, the combined teaching of the Pedersen and Trimberger references further teaches "the set of indices for each sub-network includes a graph index and a set of function indices, wherein, for each sub-network, the graph index identifies the storage location of the graph for the sub-network, and each function index identifies the storage location of a local function of the sub-network" (See Pedersen Figs. 4A-4B and col. 6, lines 29-35 and 54-59 where gates and nodes are selected from the synthesized and un-synthesized sub-netlist one by one for analysis).

As per claim 10, the combined teaching of the Pedersen and Trimberger references further teaches "the data storage structure associates the generated parameter for each sub-network with the graph and function identifier for the sub-network" (See Pedersen:

col. 11, line 62 – col. 4, line 3 where a sub-netlist is identified and synthesized for its nodes and the graph by mapping the changed design onto the target hardware).

As per claim 13, the combined teaching of the Pedersen and Trimberger references further teaches the following:

“each sub-network includes a set of circuit elements” (See Pedersen: Fig. 7A and col. 14, lines 17-32 where the netlist consists of gates, clock and registers);

“the data storage structure stores each sub-network in terms of (i) an encoding of a graph that represents the topology of the set of circuit elements of each sub-network, wherein the graph includes a node for each circuit element of the sub-network” (See Pedersen: at col. 6, lines 20-23 where electronic design is provided as a high level Boolean representation, encoded in a hardware design language and as schematic or any other form representing the logical arrangement of a device, and at col. 1, lines 37-43 referencing U.S. Patent Application 08/958,778 where Southgate states a fully described block diagram stored in a graphic design file at col. 4, lines 65-67); and

“(ii) a set of local functions that includes a local function for each node of the graph” (See Pedersen: Fig. 7E where a set of local functions include the functions at nodes u and v) ; and

“for each retrieved sub-network, the manager retrieves the graph and the set of local functions of the sub-network” (See Pedersen: Fig. 3A, step 314, and col. 10, lines 40-50 where compiler is the data access manager for identifying the sub-netlist, by a comparison process, and retrieving the sub-netlist to be incrementally recompiled).

As per claim 14, the combined teaching of the Pedersen and Trimberger references further teaches the following:

"the data storage structure stores, for each sub-network, an identifier that specifies the set of local functions and the graph" (See Pedersen: col. 11, line 62 – col. 4, line 3 where a sub-netlist is identified and synthesized for its nodes and the graph by mapping the changed design onto the target hardware);

"the data storage structure associates the generated parameter for each sub-network with the graph and function identifier for each sub-network" (See Pedersen: Fig. 3A, step 314, and col. 10, lines 40-50 where the compiler conducts a the process for identifying the sub-netlist, by a comparison process, and retrieving the sub-netlist to be incrementally recompiled); and

"the manager uses the received parameter to identify an identifier associated with the received parameter, and then uses the identified identifier to retrieve a graph and a set of local functions" (See Pedersen: Fig. 3A, step 314, and col. 10, lines 40-50 where user is allowed to input changed design for identifying the new gates such the incremental synthesized process can start).

As per claim 15, the combined teaching of the Pedersen and Trimberger references further teaches "the manager uses the received parameter to identify a set of identifiers associated with the received parameter, and then use the identified set of identifiers to retrieve graphs and sets of local functions that specify several sub-network" (See

Pedersen: Fig. 3A, step 314, and col. 10, lines 40-50 where compiler is the data access manager for identifying the sub-netlist, by a comparison process, and retrieving the sub-netlist to be incrementally recompiled).

Allowable Subject Matter

8. Claims 8-9 and 18-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. § 101 and 35 U.S.C. § 112, and in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

9. The Applicant's arguments filed on May 15, 2006 have been fully considered, but are moot on new grounds of rejection.

Conclusions

10. The prior art made of record

A. U. S. Patent No. 6,134,705

J. U. S. Patent No. 5,959,881

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

G. U. S. Patent No. 6,925,088

H. U. S. Patent No. 6,009,251

B. U. S. Patent No. 6,110,223

C. U. S. Patent No. 6,102,964

D. U. S. Patent No. 5,201,046

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E. U. S. Patent No. 5,440,720

F. U. S. Patent No. 6,272,529

I. U. S. Patent No. 5,956,257

Contact Information

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kuen S Lu whose telephone number is (571) 272-4114. The examiner can normally be reached on Monday-Friday (8:00 am-5:00 pm). If attempts to reach the examiner by telephone are unsuccessful, the examiner's Supervisor, John Cottingham can be reached on (571) 272-7079. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for Page 13 published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 886-217-9197 (toll-free).

Kuen S. Lu



Patent Examiner, Art Unit 2167

July 26, 2006